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A Low Power Hybrid Partition SRAM based TCAM with a Parity Bit

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Abstract— Ternary Content Addressable memory provides high speed search operation. When compared to RAM, TCAM suffers certain limitation like low bit density, slow access time, high cost per bit. In this paper, we introduced a parity bit to boost the searching speed HP SRAM based TCAM with less power and delay. A novel memory architecture called HP SRAM based TCAM, which emulates TCAM functionality with SRAM memory. The architecture of HP SRAM based TCAM with a parity bit was verified by VHDL in ModelSim.

Keywords— TCAM, APT, BPT, APTAG, Hybrid Partition, SRAM, ANDing operation.

I. INTRODUCTION

Ternary Content Addressable (TCAM) is a special type of memory, which receives an input search word and returns the address of that word which it is stored on its data bank [1]. TCAM search the entire contents in a single clock cycle. TCAM has the ability to store three states 0, 1, and don't care condition ("X"). It can be described as the opposite of RAM [2]. Due to its parallel nature, TCAM used a wide variety of applications such as network routers, image processing and data compression.

When compared to RAM, the cost of conventional TCAM device is high [3]. Hybrid Partitioned SRAM based TCAM achieves advantages like bit density, lower cost, and comparable search performance. HP SRAM based TCAM that emulates TCAM functionality with SRAM memory [4]. Conventional TCAM divide along vertically and horizontally and form TCAM sub tables. Each TCAM sub table is named as Hybrid Partition. All TCAM sub tables are stored in their corresponding SRAM memory units.

In this work, a parity bit is introduced to boost the searching speed of HP SRAM based TCAM with less power and delay. These newly introduced parity bits are used to find the matched word and reduce the comparison with the mismatched word. This is similar to the existing HP SRAM based TCAM, but it has a different operating principle. By this way the total power consumption in HP SRAM based TCAM is reduced when compared with already existing schemes [5]-[8].

II. ARCHITECTURE OF HP SRAM BASED TCAM

Fig. 1 illustrates an overall architecture of HP SRAM based TCAM where each layer corresponds to Fig. 2. It contains m layers and Global Priority Encoder (GPE). All layers receive input word simultaneously during searching operation. Potential Matching Address (PMA) is an output of each layer. If multiple PMA occurs, GPE select the highest priority as a Matching Address (MA). Lower layer of PMA has the highest priority.

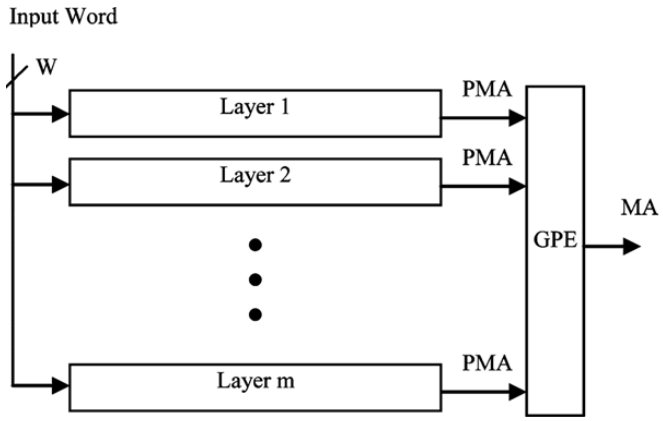

Fig. 1 Memory Architecture of HP SRAM based TCAM

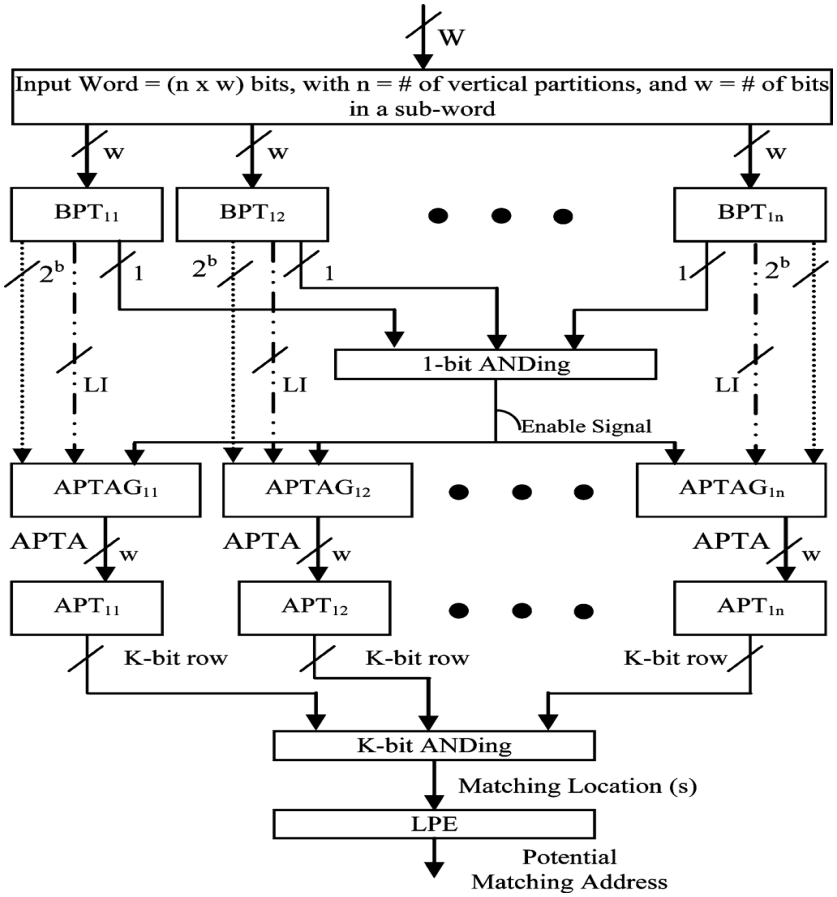

Fig. 2 Architecture of a layer of HP SRAM based TCAM

Main components are Bit Position Tables (BPTs), Address Position Tables (APTs), Address Position Table Address Generators (APTAGs), Local Priority Encoder (LPE), and ANDing operation. In BPT, 2^W bits of memory are grouped into 2^{W-b} bit of rows. Each row is supplemented with a value is called Last Index (LI) and its length is w+1 bit. The high order bits ("w-b") of input words used to select a particular row in BPT acting as an address. This address is termed as BPT Address (BPTA). The low order bits ("b") of the input sub word are used to indicate a particular bit position in the row selected and it's named as Bit Position Indicator (BPI). If BPI is high means input sub word is present. Last Index of a row is set to the total number of bits in all previous rows reduced by one. Fig. 3 shows the Conceptual view of BPT.

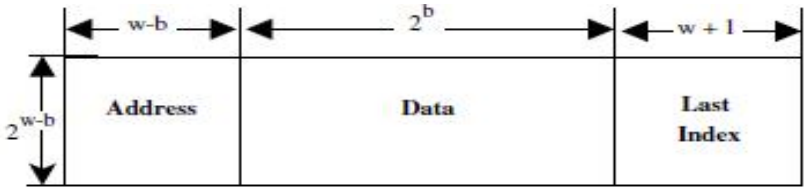

Fig. 3 Conceptual view of BPT

APTAG generates an address referred to APTA, which contains 1's counter and adder. The 1's counter counts the number of ones in the selected row of BPT and then forwards this information to adder. The adder then adds the 1's counter output and LI of the selected row. Fig. 4 shows the conceptual view of APT, where K bits represent the number of bits in each row.

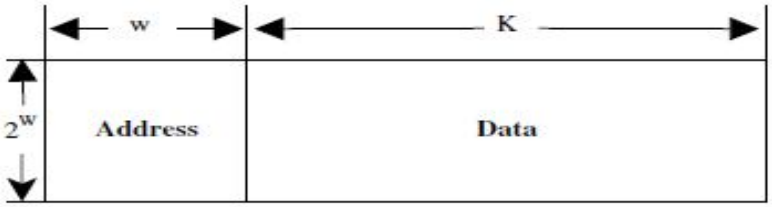

Fig. 4 Conceptual view of APT

A. Searching in HP SRAM based TCAM

During searching operation [10], an input word is applied to all layers of HP SRAM based TCAM and it's partitioned into n sub words, which are then applied to their corresponding BPTs in parallel. Upon reading, each access memory location produces a single bit ie, '1' or '0'. If read out a bit is high, an input sub word is present and sustain the search operation. Upon validation of all sub word, each sub word access a memory location in its corresponding APT and read K bits data. All the validated sub words read out their respective memory locations concurrently from their corresponding APT, which are then bit-wise ANDed. LPE receives the K-bit AND operation result and selects PMA. GPE select MA from the multiple PMA.

B. Searching in HP SRAM based TCAM with a Parity Bit

The new architecture has the same interface as the conventional HP SRAM based TCAM with one extra bit. The proposed TCAM with a parity bit design consisting of the original data segment and an extra one bit segment derived from the actual data bits. Parity bit is either odd or even. The extractor is used to find the parity bit value. During the search operation, the matched parity bit value of word is found first. Only the word whose parity bit value matched will be compared with the search word and reduce the comparison with the mismatched word [9].

III. RESULTS

A. Simulation Result

The performance analysis HP SRAM based TCAM architecture is analysed and it is simulated using ModelSim simulator in Fig. 5. Also HP SRAM based TCAM with a parity bit is analysed as shown in Fig. 6.

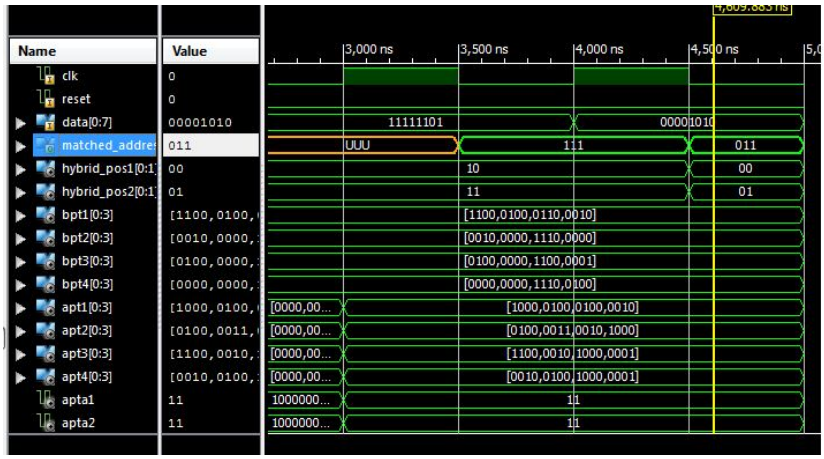

Fig. 5 Simulated Waveform of HP SRAM based TCAM

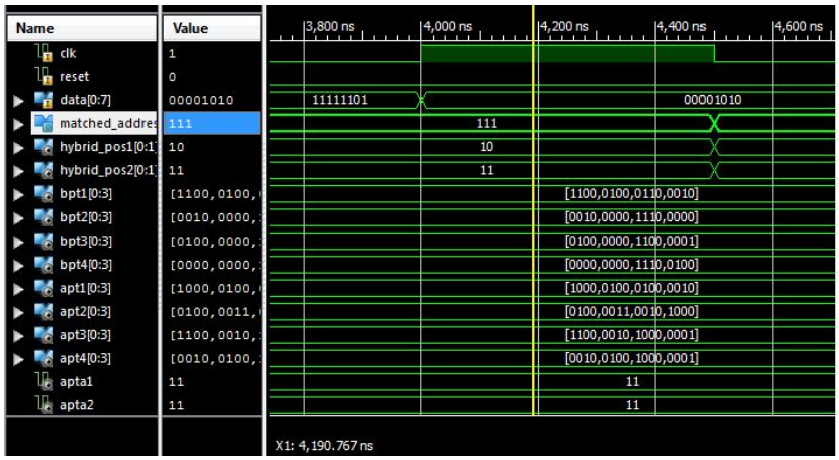

Fig. 6 Simulated Waveform of HP SRAM based TCAM with a Parity Bit

B. Synthesis Results

Using Xilinx ISE 13.1, synthesis is done and analysed. The synthesis report is gives the parameters enhanced like power dissipation and delay.

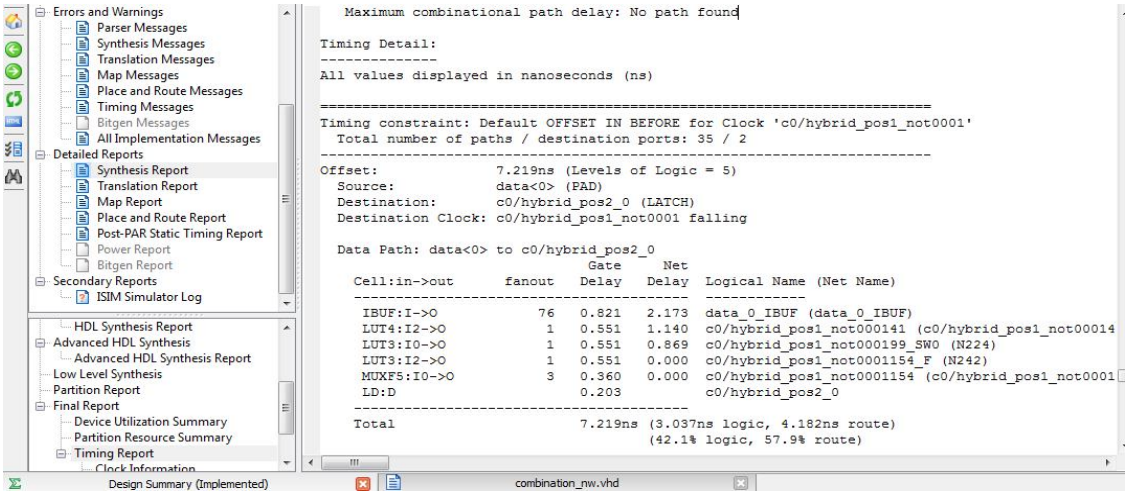

Fig. 7 Delay of HP SRAM based TCAM

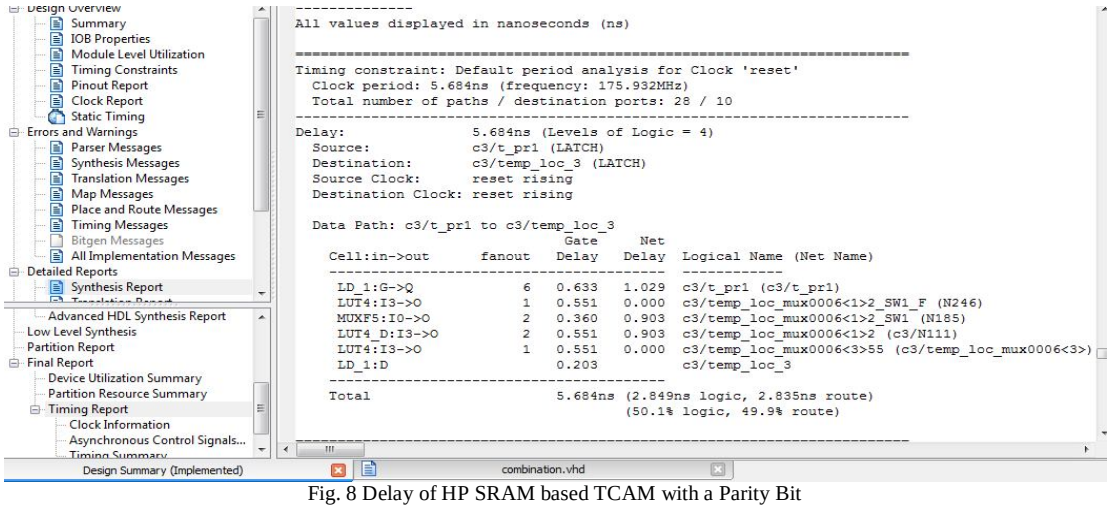

Fig. 8 Delay of HP SRAM based TCAM with a Parity Bit

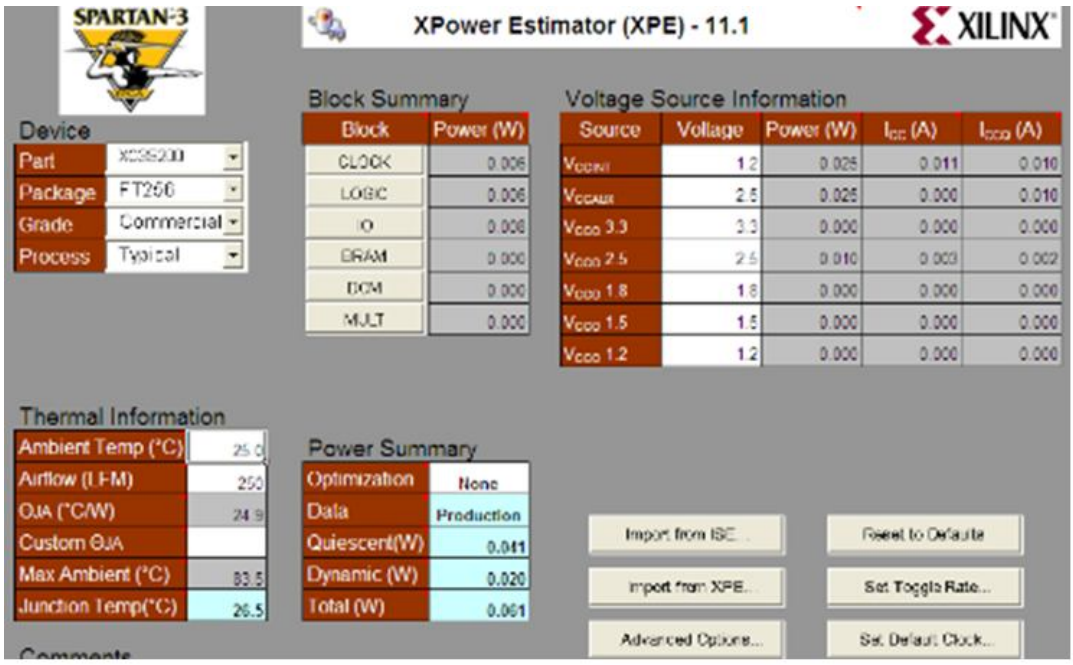

Fig .9 Power of HP SRAM based TCAM

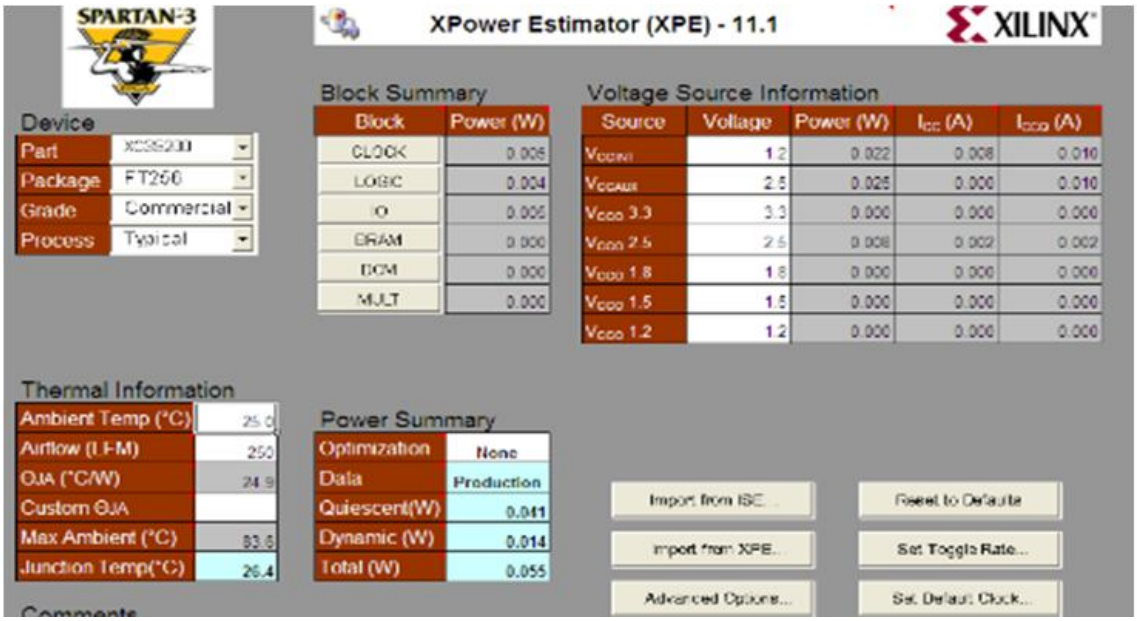

Fig. 10 Power of HP SRAM based TCAM with a Parity Bit

C. Results Comparison

TABLE I shows that HP SRAM based TCAM with a parity bit has given the better performance compared to existing method.

TABLE I
COMPARISON OF HP SRAM BASED TCAM AND HP SRAM BASED TCAM WITH A PARITY BIT

Parameter	Delay (ns)	Power (mW)	Power*Delay (J)
HP SRAM based TCAM	7.219	61	4.49E-10
HP SRAM based TCAM with a Parity Bit	5.684	55	3.12E-10

IV. CONCLUSIONS

We proposed a low power TCAM with high speed. It support large input patterns with much simpler design structure, and has a deterministic search performance. The proposed design has a low power dissipation and shorter propagation delay compared to existing method.

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REFERENCES

[1] S. Baeg, "Low power ternary content-addressable memory design using a segmented match line, "*IEEE Trans. Circuits Syst. I*, vol.55, no.6, pp. 1485-1494, Jul.2008.
[2] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: A tutorial and survey," *IEEE J. Solid State Circuits*, vol. 41,n0. 3,pp. 712-727, Mar. 2006.
[3] P. Mahoney, Y. Savaria, G. Bois, and P. Plante, "Performance characterization for the implementation of content addressable memories based on parallel hashing memories," *P. Stentrom (ED.): Trans. HiPEAC II, LNCS 5470*, pp.307-325, 2009.
[4] Zahid Ullah, Kim Ilgon, and Sanghyeon baeg, "Hybrid partitioned SRAM-based ternary content addressable memory," *IEEE Trans. Circuits Syst. I*, vol. 59, no.12, pp. 2969-2978, Dec. 2012.
[5] Anh-Tuan Do, Shoushun Chen, Zhi-Hui Kong, and Kiat Seng Yeo, "A high speed low power CAM with a parity bit and power-gated ML sensing," *IEEE Trans. Very Large Scale Integration (VLSI) System*, vol. 21, no. 1, pp. 151-156, Jan. 2013.
[6] K. Pagiamtzis and A. Sheikholeslami, "A low-power content- addressable memory (CAM) using pipelined hierarchical search scheme," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1512-1519, Sep. 2004.
[7] I. Arsovski and A, Sheikholeslami, "A mismatch-dependent power allocation technique for matchline sensing in content-addressable memories," *IEEE J. Solid-State Circuits*, vol.38, no. 11, pp. 1958-1966, Nov. 2003.
[8] J. Chang, "Using the dynamic power source technique to reduce TCAM leakage power," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 11, pp. 888-892, Nov. 2010.
[9] Do, S. S. Chen, Z. H. Kong, and K. S. Yeo, "A low-power CAM with efficient power and delay trade-off," in *Proc. IEEE int. Symp. Circuits Syst. (ISCAS)*, 2011, pp. 2573-2576.
[10] B. D. Yang, Y. K. Lee, S. W. Sung, J. J. Min, J. M. Oh, and H. J. Kang, "A low power content addressable memory using low swing search lines," *IEEE Trans. Circuits Syst. I*, vol.58, no. 12, pp. 2849-2858, Dec. 2011.

